What is claimed is:

1. A semiconductor device comprising:

a support semiconductor chip;

first and second chip blocks supported and connected on one surface of the support semiconductor chip and each including one or a plurality of semiconductor chips having an active surface substantially parallel with the one surface of the support semiconductor chip;

an insulator arranged between the first and second chip blocks; and

an intralevel wiring arranged within or on a surface of the insulator, on a wiring plane as a plane including an inactive or active surface of any of the semiconductor chips constituting the first or second chip blocks.

2. A semiconductor device according to claim 1, wherein the active or inactive surface of any of the semiconductor chip constituting the first chip block and the active or inactive surface of any of the semiconductor chip constituting the second chip block are commonly on the wiring plane.

3. A semiconductor device according to claim 1, wherein the intralevel wiring includes first and second intralevel wirings respectively arranged on first and second wiring planes not in a same plane, further including an interlevel wiring connecting between the first and second intralevel wirings.

4. A semiconductor device according to claim 1, wherein at

least one of the semiconductor chips constituting the first and second chip blocks has a penetration hole arranged with a conductor therein.

5. A method for manufacturing a semiconductor device including:

a step of connecting, to one surface of a support semiconductor chip, first and second chip blocks each including one or a plurality of semiconductor chips having an active surface substantially parallel with the one surface of the support semiconductor chip;

a step of arranging an insulator at between the first and second chip blocks; and

a step of forming, within or on a surface of the insulator, an intralevel wiring on a wiring plane as a plane including an inactive or active surface of any of the semiconductor chips constituting the first or second chip block.

6. A method for manufacturing a semiconductor device according to claim 5, wherein the active or inactive surface of any of the semiconductor chip constituting the first chip block and the active or inactive surface of any of the semiconductor chip constituting the second chip block are commonly on the wiring plane.

7. A method for manufacturing a semiconductor device according to claim 5, wherein the step of forming the intralevel wiring includes a step of forming first and second intralevel

wirings respectively arranged on first and second wiring planes not in a same plane, further including a step of forming an interlevel wiring connecting between the first and second intralevel wirings.

8. A method for manufacturing a semiconductor device according to claim 5, further including a step of forming a penetration hole in at least one of the semiconductor chips constituting the first and second chip blocks, and a step of arranging a conductor in the penetration hole.

9. A method for manufacturing a semiconductor device including:

an on-substrate connecting step of connecting face down a semiconductor chip having an active surface formed with a recess arranging a conductor therein onto an one surface of a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to expose the conductor in the inactive surface of the semiconductor chip after the on-substrate connecting step.

10. A method for manufacturing a semiconductor device according to claim 9, wherein the semiconductor substrate is a semiconductor wafer, the on-substrate connecting step including a step of arranging and connecting the semiconductor chips in plurality side by side on a semiconductor wafer, further including a step of cutting the semiconductor wafer based on

a predetermined region including at least one of the semiconductor chips to obtain a semiconductor device having a chip-on-chip structure.

11. A method for manufacturing a semiconductor device according to claim 9, wherein the one surface of the semiconductor substrate is an active surface, further including a substrate polish step of polishing or abrading the inactive surface of the semiconductor substrate to reduce the thickness thereof.

12. A method for manufacturing a semiconductor device according to claim 11, wherein the semiconductor substrate has an active surface formed with a recess arranging a conductor therein, the substrate polish step including a step of polishing or abrading the inactive surface of the semiconductor substrate to expose the conductor of the semiconductor substrate in the inactive surface of the semiconductor substrate.

13. A method according to claim 9, further including an on-chip connecting step of connecting, on the semiconductor chip, another semiconductor chip.

14. A method according to claim 13, wherein the other semiconductor chip has an active surface formed with a recess arranging a conductor therein, the on-chip connecting step being to connect face down the other semiconductor chip on the semiconductor chip, further including a step of polishing or abrading an inactive surface of the other semiconductor chip to expose the conductor of the other semiconductor chip in the

inactive surface of the other semiconductor chip.

15. A method for manufacturing a semiconductor device including:

a step of connecting a semiconductor chip on an active surface of a semiconductor substrate having an active surface formed with a recess arranging a conductor therein; and

a step of polishing or abrading an inactive surface of the semiconductor substrate to expose the conductor of the semiconductor substrate in the inactive surface of the semiconductor substrate.

16. A method for manufacturing a semiconductor device including:

an on-substrate connecting step of connecting a semiconductor chip face down on a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to reduce a thickness of the semiconductor chip after the on-substrate connecting step.

17. A semiconductor device having a structure superposed with a plurality of semiconductor chips, wherein at least one of the semiconductor chips has a penetration hole arranging a conductor therein and penetrating the semiconductor chip in the thickness direction.

18. A semiconductor device according to claim 17, wherein the plurality of semiconductor chips include a first semiconductor chip having a first penetration hole arranging a conductor

therein and a second semiconductor chip superposed adjacent to the first semiconductor chip and having a second penetration hole arranging a conductor therein in a position deviated from the first penetration hole.